Digital Backend for JPL Deep Space Communications Complex VLBI Processor

Casper Workshop 2010

Robert Navarro*

Doug Wang*

Melissa Soriano*

Les White*

Eric Clark*

Elliott Sigman*

Chris Jacobs*

* Jet Propulsion Laboratory, California Institute of Technology.

JPL VLBI Roadmap

- VLBI Systems for Radio Reference Frame and Time & Earth Motion Precision Observations:
  - Replace aging VLBI Data Acquisition Terminal hardware (based on MarkIV hardware) with modern Digital Backend based system (new JPL VLBI Processor).
  - At the same time, upgrade to Mark5C disk packs for data storage.
  - Make incremental improvements to JPL VLBI Software Correlator to support Mark5C hardware and data formats.
  - Maintain compatibility with other VLBI centers for DSN support of Host Country activities.
- VLBI Systems for Double Differential One Way Ranging
  - Incremental upgrades to Wideband VLBI Science Receiver (WVSR).
  - WVSR optimized for narrow band processing. (But, modified version of channelization firmware planned for JPL Roach Board firmware).
  - Developed initially for radio science experiments. Can follow spacecraft frequency predicts to millihertz accuracy.
- Long Term Goal is to have flexible JPL digital backend system that can handle both tasks. Moving to Digital Backend hardware based on Roach board gets us closer to goal, but not all the way there.
  - Different requirements, operating modes, file formats, system interfaces require two systems for now.
  - Current & future ROACH based platforms are a good fit, but there are program pressures to find and choose a common COTS vendor for future VLBI, Arraying, Telemetry digital backends.

Plans for Modernized JPL Digital Backend for Deep Space Network Applications

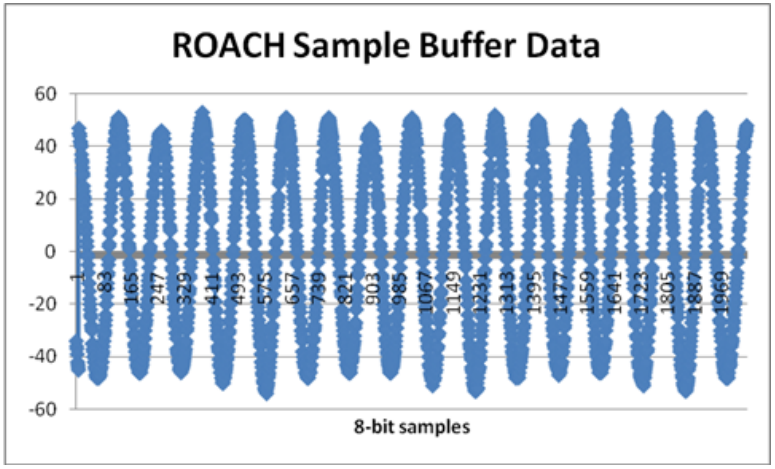
- Plan is for two IF system to cover up to 500 GHz of bandwidth.
- An IF Switch will handle up to 10 IF inputs.
- Sampling Bandwidth of each IF is 640 MHz but 1dB bandwidth of each system after anti-aliasing filters is 500 MHz
- Accepts DSN IF input band of 100-600 MHz. Good for S band (2.3 GHz), X band (8.4 GHz) and Ka band (31.2 GHz)
- Planning on using JPL developed IF sampler module, CASPER ROACH board for Digital Processing and Channelization and Mark5C disk recorders.
- Using DSN based Wideband VLBI Science Receiver as underlying basis of system control software and develop VEX interface layer on top of that structure.
  - Need to interface to JPL Deep Space Network monitor & control infrastructure.

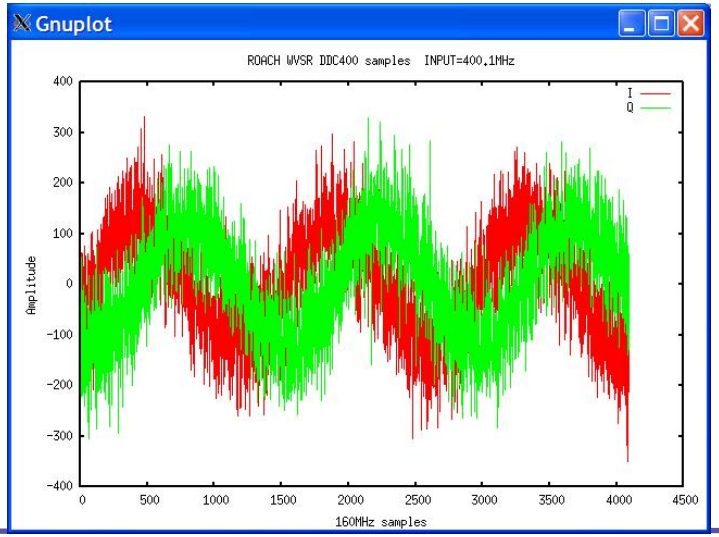
Implementation Details and Heritage

- Large code base (software, firmware) from previous generation open loop digital receiver (WVSR) available for porting.
- Similar hardware (PPC440GX & Virtex2Pro versus PPC440EPx and Virtex5) makes porting feasible.
- Desire using optically isolated 1280 MHz ADC module developed for WVSR for radio science experiments & space craft searches that require very low noise spurs with ROACH board. Requires transition module. Transition module has form factor of iADC boards.
- Previous PPC440Gx software developed using memory mapped device driver. Need this to run on ROACH with no special modifications to ROACH kernel.
- Previous Virtex2Pro FPGA firmware developed in mix of Verilog and System Generator. Want to port over to Roach while keeping same basic memory map format.

Current Progress for JPL VLBI Processor Digital Back End

- Transition board from JPL sampler to ROACH board complete.
- Raw samples 1280 MHz digitized samples captured over Digitizer to ROACH interface board.
- Software and firmware from WVSR platform (based on PPC440GX and Virtex2 Pro FPGAs) ported to ROACH platform.
- Usage of Linux memory mapped drivers for PPC440GX sucessfully tested on ROACH.
- Firmware for digital downconversion filters ported to Virtex5 architecture and has been partially tested.





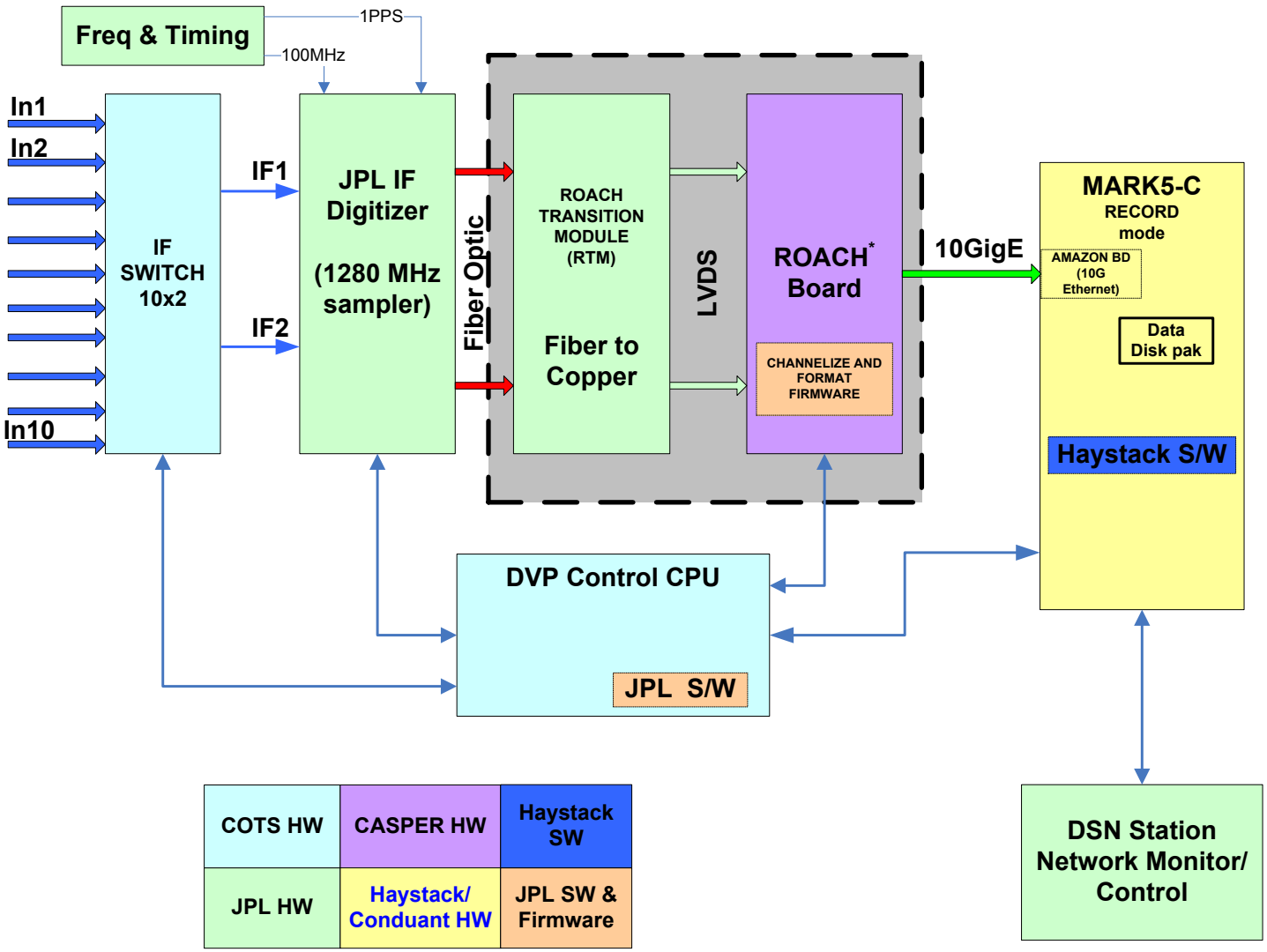
Requirement Highlights for JPL VLBI Processor

- IF Input Bandwidth = 100 to 600 MHz (500 MHz Bandwidth)
- IF inputs to simultaneously process = 2
- Number of channels = 16 for VLBI Data, 4 to 8 for phase cal
- Format of channels = Upper and Lower Sideband, In-Phase and Quadrature-Phase (complex)
- Supported Channel Bandwidths = 32MHz to 1 KHz (64 MHz possibly)
- Supported bits per channel = 8, 4, 2 or 1 bits per sideband.

Block Diagram of new JPL VLBI Processor Digital Back End

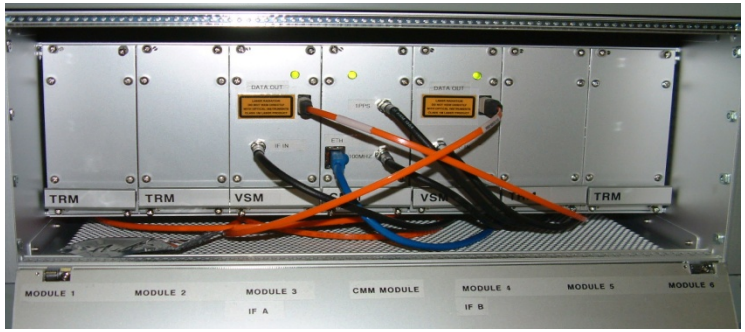
Jet Propulsion Laboratory
California Institute of Technology

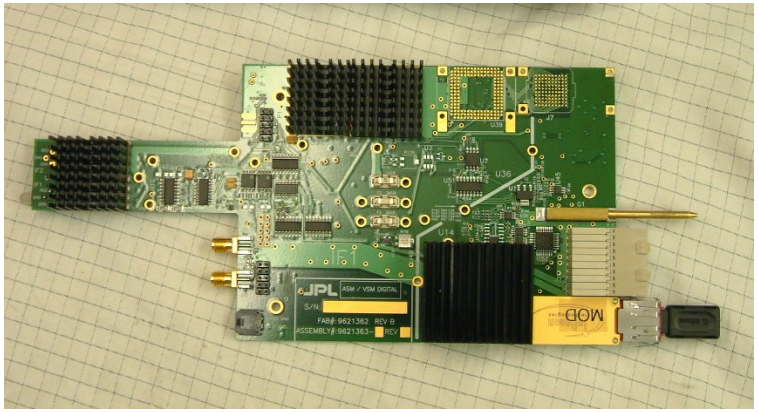
JPL Deep Space Communication Complex VLBI Processor (DVP)



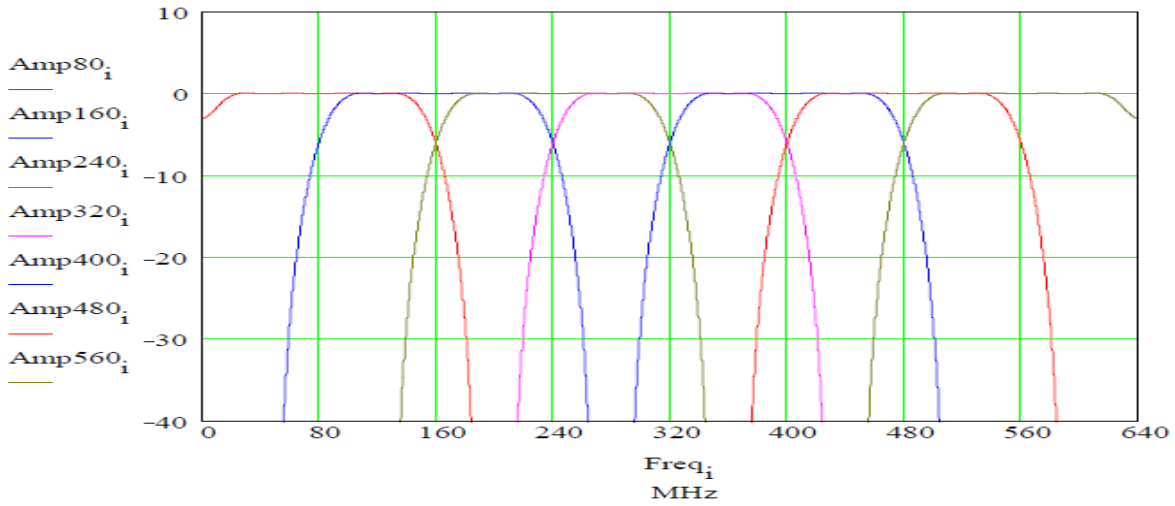
Details on JPL IF Digitizer Module

- Already in operational use at DSN
- Atmel (e2V) A/D samples 8 bits at 1280 MHz
- Usable band of 100 to 600 MHz or 700 to 1200 MHz
- Digitally controlled built-in attenuator
- Optically isolated from digital processing back ends.
  - Spurious signals attenuated 97 dB below A/D saturation level.
  - Enables use for spectral line work
- Generates 1280 MHz sampling clock from 100 MHz reference
- Uses interface module to connect to Roach Board.





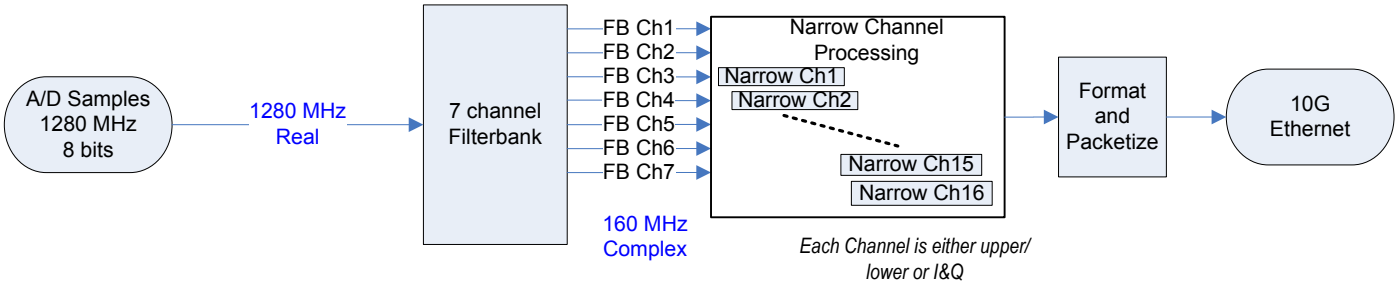
JPL Channelization FPGA firmware



- JPL VLBI DAT Digital Backend Channelization broken up into two stages
- First stage of VLBI DAT channelization processing breaks input signal up into 7 fixed bands of data, each 160 MHz (complex).
- Each band is 80 MHz apart on center.
- Each band overlaps other bands by 80MHz on a side.
- One instance of 1st stage per IF
- Second stage selects one of eight first stage wideband inputs. Then applies digital mixer for precise channel location selection. Cascade of downconverting filters provides variable output bandwidth per channel (32 to 1KHz)
- Sixteen instances of second stage

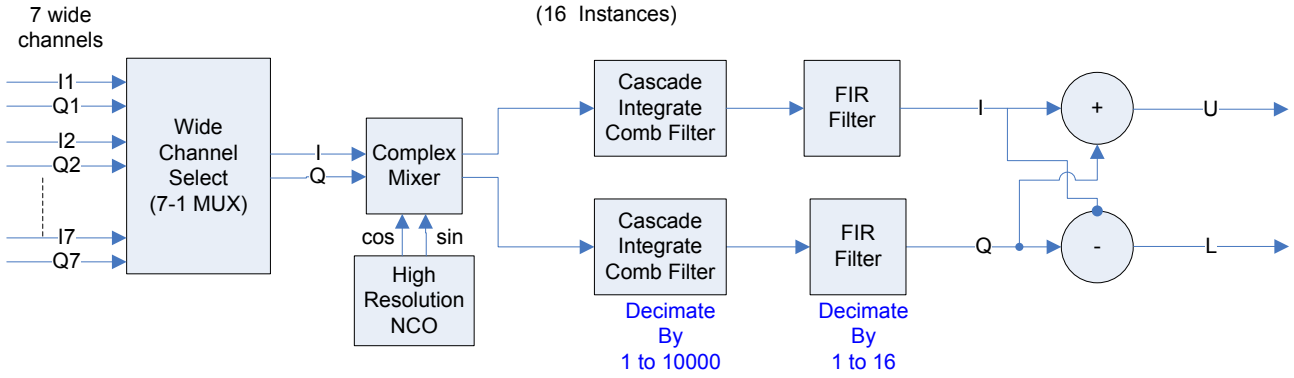
JPL VLBI Processor Digital Back End Firmware Architecture

Wideband Processing:
First Stage Downconvertion
Using polyphase Filterbank



Narrow Channel Processing

32 MHz to 1 KHz
(16 Instances)



Summary

- NASA Deep Space Network navigation requirements are main driver for modernization of VLBI data acquisition equipment at JPL
  - Improve system sensitivity (higher bandwidths), maintainability, accuracy and flexibility.
- Support non-DSN customers at Deep Space Network sites.
- Maintain compatibility with Haystack Mk5 systems.
- Maintain expertise and flexibility to make modifications for internal customers and science experiments.
- Leverage off developments in VLBI community