Dual 8bit 1 Gsps ADC
Replacing
AT84AD001B with AT84AD001C

Application Note

1. Introduction

The aim of this application note is to highlight the differences between the two revisions of Dual 8 bit 1 Gsps ADC: AT84AD001B and AT84AD001C and provide the recommendation for an easy migration.

The AT84AD001B and AT84AD001C are fully pin to pin compatible at package level with same footprint and same mechanical characteristics.
The AT84AD001C is an improved version of AT84A001B the two products are very close to allow an easy upgrade on all applications developed with AT84AD001B.

The main improvements between the AT84AD001B and the AT84AD001C are:
• BER
• SNR and ENOB
• Crosstalk
• Timing centering of Output Clock versus Output Data

The main differences between the AT84AD001B and the AT84AD001C are:
• Gray mode not available
• Inverted selection of Output Clock rate Fs/2 or Fs/4 in DMUX1:2
• Pipe line delay
• Slight increase of power supply current

This migration document applies to both packages: LQFP 144 (leaded) and LQFP-ep 144 (green package):

• AT84AD001BCEPW → AT84AD001CCEPW (LQFP-ep 144 green package C grade)
• AT84AD001BVEPW → AT84AD001CVEPW (LQFP-ep 144 green package V grade)
• AT84AD001BCTD → AT84AD001CCTD (LQFP 144 C grade)
• AT84AD001BITD → AT84AD001CVTD (LQFP 144 V grade)

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2. Comparing AT84AD001B and AT84AD001C

2.1 Performances

Parameter	AT84AD001B	AT84AD001C	Migration recommendation
BER sinewave Fin=250MHz (-1dBFS)	10^{-13} @ Fs=800Msps	**10^{-13}** **@ Fs=1Gsps**	
BER Middle code glitch occurrence @ Fs=1Gsps DC signal at mid scale	Typical 10^{-8}	**Typical 10^{-12}**	
Crosstalk (at 250Mhz)	-55 dB	**-65 dB**	
Dynamic performance Normal mode Fs = 1Gsps, -1 dBFS Fin = 500MHz SNR typical ENOB typical Fin=1GHz SNR typical ENOB typical	 42 dB 6.8 bit 41 dB 6.4 bit	 **45 dB** **7.2 bit** **43 dB** **7.0 bit**	
Typical power supply current DMUX 1:1 Ivcca Ivccd Ivcco	 150 mA 230 mA 100 mA	 145 mA **248 mA** 88 mA	Check that power supplies Vccd support new current values
Typical power supply current DMUX 1:2 and 1 clock Ivcca Ivccd Ivcco	 150 mA 260 mA 175 mA	 145 mA **272 mA** 154 mA	Check that power supplies Vccd support new current values
Typical power supply current DMUX1:2 and 2 clocks Ivcca Ivccd Ivcco	 150 mA 290 mA 180 mA	 145 mA **296 mA** 158 mA	Check that power supplies Vccd support new current values
Typical power supply current Full Standby Ivcca Ivccd Ivcco	 12 mA 24 mA 3 mA	 14 mA 20 mA 4.3 mA	
Typical power dissipation DMUX 1:1	1.4 W	**1.5 W**	Check board to support new power dissipation values

2.2 Features and serial interface settings

Feature	AT84AD001B	AT84AD001C	Migration recommendation
Gray mode D2 at address 000	Available	**Not supported**	Check if Gray mode used. If yes, switch output Data to Binary format in ADC and change FPGA program to convert Gray code into Binary code.
Data Ready setting DMUX 1:2 D14=0 at address 000 (default value) D14=1 at address 000	 CLKOI&Q = Fs/2 CLKOI&Q = Fs/4	**Inverted** **CLKOI&Q = Fs/4** **CLKOI&Q = Fs/2**	If mode DMUX 1:2 used, change serial interface setting.
ISA recommended setting DMUX 1:1 DMUX 1:2 [D2- D0]-[D6- D6] at address 100	 -50 ps -50 ps	 **0 ps** **-100 ps**	Change serial interface setting to optimize ADC dynamic performance.
DRDA Tuning (Data Ready Delay Adjust) Range Step [D2- D0]-[D6- D6] at address 111	 -560 to +420 ps 140 ps	 **-340 to +255 ps** **85 ps**	Check and retune, if needed, the ADC to FPGA communication timings.
FiSDA Tuning (Fine Sampling Delay Adjust) Range Step [D10- D6] at address 111	 -64 to +120 ps 8 ps	 **-60 to +60 ps** **4 ps**	If FiSDA used for interleaving mode, recheck the SDA fine tuning process.
Built-in Test mode ramp active ADC I ADC Q	Need CLKI or CLKQ for ADC I CLKI or CLKQ for ADC Q	**Need** **CLKI for ADC I** **CLKQ for ADC Q**	Adapt application if ramp must be used
Built-in Test mode ramp active Maximum clock rate DMUX 1:1 Data change every DMUX 1:2 Data change every D1 at address 110	 750 Msps clock cycle 2 clock cycles	 **1 Gsps** **2 clock cycles** **2 clock cycles**	Adapt FPGA if Built-in Test mode active and ramp used in DMUX 1:1.
Chip version test bit D2 at address 000	Not available	**Available** **Chip version test bit active bit D2=0** **➔ Output bit CAL change to high level**	

2.3 Timings

Parameter	AT84AD001B	AT84AD001C	Migration recommendation
Output data clock centering versus output data DMUX 1:1	Not always centered. (Fixed delay between clock and data)	**Clock always centered versus data (rising and falling edge)**	Check and, if needed, retune the ADC to FPGA communication timings.
Output data clock centring versus output data DMUX 1:2 and Fs/4	Not always centered. (Fixed delay between clock and data)	**Clock always centered versus data (rising and falling edge)**	Check and, if needed, retune the ADC to FPGA communication timings.
Pipeline delay Nominal mode DMUX 1:1: Port A DMUX 1:2: Port A DMUX 1:2: Port B	 3.5 4 3	 **5** **5** **4**	Adapt application if sensitive to pipeline delay.
Pipeline delay Transparent T/H mode DMUX 1:1: Port A DMUX 1:2: Port A DMUX 1:2: Port B	 3 3.5 2.5	 **4.5** **4.5** **3.5**	Adapt application if sensitive to pipeline delay.
DDRB Reset		DDRB reset is needed whenever the following functions are changed: **DMUX mode FS/2 – FS/4 function**, **clock frequency**	Adapt application if this function are changed (DDRB reset mandatory)
Aperture delay : TA	1ns	**0.8ns**	Adapt application if sensitive to aperture delay.

Note: the rising edge of Output Clock in DMUX 1:2 and Fs/2 mode is always centred on output data in both AT84AD001B and AT84AD001C

3. Application Information

This section discusses the implementation of changes described above.

3.1 Gray mode and Chip version test bit

AT84AD001B
Serial interface setting at address '000': bit D2

Table 3-1. Gray

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	X	X	X	X	X	X	Binary/Gray	X	X

Binary mode bit D2=1 (default value)
Gray mode bit D2=0

AT84AD001C
Serial interface setting at address '000': bit D2

Table 3-2. Chip version

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	X	X	X	X	X	X	ChipVersion	X	X

Chip version test bit inactive bit D2=1 (default value)
Chip version test bit active bit D2=0 ➔ Output bit CAL change to high level

3.2 Internal setting Adjustment (ISA) recommended setting

Recommended setting for optimal setting

Serial interface setting at address '100'

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	0	0	Channel Q			Channel I		

Table 3-3. ISA

Mode	AT84AD001B value	Programming D2 to D0 and D5 to D3	AT84AD001C value	Programming D2 to D0 and D5 to D3
DMUX 1:1	-50 ps	011	0 ps	100 (default value)
DMUX 1:2	-50 ps	011	-100 ps	010

3.3 Output Clock data rate Fs/2 or Fs/4

AT84AD001B
Serial interface setting at address '000': bit D14

Table 3-4. Fs/2 or F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	OutputDataRate	X	X	X	X	0	X	X	X	X	X	X	X	X	X

Fs/2 Output clock Data Rate D14 = 0 (default value)
Fs/4 Output clock Data Rate D14 = 1

AT84AD001C
Serial interface setting at address '000': bit D14

Table 3-5. Fs/4 or Fs/2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	OutputDataRate	X	X	X	X	0	X	X	X	X	X	X	X	X	X

Fs/4 Output clock Data Rate D14 = 0 (default value)
Fs/2 Output clock Data Rate D14 = 1

3.4 Data ready Delay Adjust (DRDA)

Serial interface setting at address '111'

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	Channel Q			Channel I		

Table 3-6. DRDA

Programming D2 to D0 and D5 to D3	AT84AD001B value Step 140 ps	AT84AD001C value Step 85 ps
000	-560 ps	-340 ps
100 (default value)	0 ps	0 ps
111	420 ps	255 ps

3.5 Fine Sampling Delay Adjustment (FiSA) on channel Q

Serial interface setting at address '111'

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	Channel Q					X	X	X	X	X	X

Table 3-7. FiSA

Programming D10 to D6	AT84AD001B value Steps 8 ps	AT84AD001C value Step 4 ps
11000	-64 ps	-60 ps
0000 (default value)	0 ps	0 ps
01111	120 ps	60 ps

How to reach us

Home page: www.e2v.com

Sales Office:

Northern Europe
e2v ltd
106 Waterhouse Lane
Chelmsford
Essex CM1 2QU
England
Tel: +44 (0)1245 493493
Fax: +44 (0)1245 492492
E-Mail: enquiries@e2v.com

Southern Europe
e2v sas
16 Burospace
F-91572 Bièvres
Cedex
France
Tel: +33 (0) 1 60 19 55 00
Fax:+33 (0) 1 60 19 55 29
E-Mail: enquiries-fr@e2v.com

Germany and Austria
e2v gmbh
Industriestraße 29
82194 Gröbenzell
Germany
Tel: +49 (0) 842 410 570
Fax:: +49 (0) 842 284 547
E-Mail: enquiries-de@e2v.com

Americas
e2v inc.
4 Westchester Plaza
Elmsford
NY 10523-1482
USA
Tel: +1 (914) 592 6050
Fax:: +1 (914) 592-5148
E-Mail: enquiries-na@e2v.com

Asia Pacific
e2v ltd
11/F,
Onfem Tower,
29 Wyndham Street,Central,
Hong Kong

Tel: +852 3679 364 8/9
Fax: +852 3583 1084
E-Mail: enquiries-ap@e2v.com

Product Contact:
e2v
Avenue de Rochepleine
BP 123 - 38521 Saint-Egrève Cedex
France
Tel: +33 (0)4 76 58 30 00
Hotline:
hotline-bdc@e2v.com